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EXAMINER
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

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	Application No.	Applicant(s)
	10/563,995	MILANESI, ANDREA
Office Action Summary	Examiner	Art Unit	
	LILIANA CERULLO	2629	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE <u>3</u> MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.
- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *14 January 2011*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-17* is/are pending in the application.

    4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-17* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

    Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

    Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

    a)☐ All b)☐ Some * c)☐ None of:

      1.☐ Certified copies of the priority documents have been received.

      2.☐ Certified copies of the priority documents have been received in Application No. _____.

      3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

    * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1)☒ Notice of References Cited (PTO-892)

2)☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)

3)☐ Information Disclosure Statement(s) (PTO/SB/08)
    Paper No(s)/Mail Date _____.

4)☐ Interview Summary (PTO-413)
    Paper No(s)/Mail Date. _____ .

5)☐ Notice of Informal Patent Application

6)☐ Other: _____ .

DETAILED ACTION

In an amendment dated, 1/14/2011, the Applicant amended claims 1, 10 and 14;

and added new claims16-17. Currently claims 1-17 are pending.

Claim Rejections - 35 USC § 103

1.   The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all

obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2.   **Claims 1, 3-10, 12 and 14-17** are rejected under 35 U.S.C. 103(a) as being

unpatentable over Tsuchi in US 2003/0160749 in view of Sakurai et al. in US 5,384,548

(hereinafter Sakurai).

3.   Regarding **claim 1**, Tsuchi discloses an apparatus comprising an input stage

(Fig. 1) with an NMOS transistor doublet *(Fig. 1 and para. 139, N-channel transistors*

103 and 104) having a first differential input *(Fig. 1 and para. 140, VinP and VinM*

toward transistors 103 and 104), for receiving input signals *(Vin per para. 141)*, a PMOS

transistor doublet *Fig. 1 and para. 139, P-channel transistors 101 and 102)* having a

second differential input *(Fig. 1 and para. 140, VinP and VinM toward transistors 101*

and 102) for receiving input signals *(Vin per para. 141)*, and a plurality of switches (*Fig.*

1, switches 111-120) for receiving and selectively directing analog input signals (*para.*

258 explain that the circuit is used for analog grayscale level voltage. Note that while

they mention Figs. 5, 8, 10 and 12. All of them incorporate the circuit shown in Fig. 1)

only to one of either said first differential input or said second differential input (*para.*

141 explains that either of the P-channel transistor pair or N-channel transistor pair

would operate as the differential pair at a time. Two types of connections are shown in

Figs. 3A-B) responsive to a switching signal (*A changeover signal is required to activate*

the switches 111-120 as required for Figs. 2-3B) and for connecting the other one of the

first and second differential inputs to a reference voltage responsive to the switching

signal *(Figs. 3A-B, where the reference voltages are Vss and Vdd. For example, in Fig.*

3A, when Vin is being supplied to the N-channel transistor pair 103 and 104 as the

differential pair, the P-channel transistor pair is acting as the current mirror and

connected to Vdd and Vss. Vice versa for Fig. 3B).

Tsuchi does not disclose details about the transconductance of the transistors.

However, Sakurai discloses the concept of keeping the ratio of the transconductance of

the NMOS transistor doublet and the transconductance of the PMOS transistor doublet

constant *(Fig. 10, where gmn is the NMOS transistor doublet transconductance and*

gmp is the PMOS transistor doublet transconductance. In the range from about 0.6Vcm

to 1.5Vcm, both gmp and gmp are constant per col. 2 lines 32-36; consequently, their

ratio gmn/gmp would be constant. Please note that there are no requirements in the

claim to maintain the ratio constant over the whole common mode range). Thus, it

would have been obvious to one of ordinary skill in the art at the time of the invention,

given that Tsuchi's differential circuit (*Tsuchi, Fig. 1*) and Sakurai's conventional OpAmp

are equivalent (*Sakurai, Fig. 1 and col. 1 lines 11-25, in that both include P-transistors*

and N-transistors pairs and act as differential input stage), to obtain the predictable

result of the ratio of the transconductance of the NMOS transistor doublet and the

transconductance of the PMOS transistor doublet to be constant, at least over a region

of the common mode voltage (*as taught by Sakurai in Fig. 10 for the range of 0.6Vcm to

1.5Vcm and col. 2 lines 32-36*) in Tsuchi's circuit (*Tsuchi, Fig. 1*).

4.   Regarding **claim 3**, Tsuchi in view of Sakurai disclose wherein the NMOS

transistor doublet comprises two NMOS transistors *(Tsuchi, Fig. 1 and para. 139, N-

channel transistors 103 and 104),* each having a gate *(as shown),* whereby the gate of

the first of the two NMOS transistors *(Tsuchi, Fig. 1, e.g. 103)* is connectable to a first

input node *(Tsuchi, Fig. 1, VinP)* via a first switch of the plurality of switches *(Tsuchi,

Fig. 1, switch 116)* and the gate of the second of the two NMOS transistors *(Tsuchi, Fig.

1, e.g. 104)* is connectable to a second input node *(Tsuchi, Fig. 1, VinM)* via a second

switch of the plurality of switches *(Tsuchi, Fig. 1, switch 117),* the PMOS transistor

doublet comprises two PMOS transistors (*Tsuchi, Fig. 1 and para. 139, P-channel

transistors 101 and 102),* each having a gate *(as shown),* whereby the gate of the first of

the two PMOS transistors *(Tsuchi, Fig. 1, e.g. 101)* is connectable to the first input node

(Tsuchi, Fig. 1, VinP) via a third switch of the plurality of switches *(Tsuchi, Fig. 1, switch

114)* and the gate of the second of the two PMOS transistors *(Tsuchi, Fig. 1, e.g. 102)* is

connectable to the second input node *(Tsuchi, Fig. 1, VinM)* via a fourth switch of the

plurality of switches *(Tsuchi, Fig. 1, switch 115).*

5.   Regarding **claim 4**, Tsuchi in view of Sakurai disclose wherein the gate of the

first of the two NMOS transistors *(Tsuchi, Fig. 1, transistor 103)* is connectable, via a

fifth switch of the plurality of switches *(Tsuchi, Fig. 1, switch 120)*, to a first reference

node being biased with a first reference voltage *(Tsuchi, Fig. 1, VSS, which is biased*

with a low-potential power voltage. As shown in Fig. 3B, during connection 2, switch

120 is ON and connects the gate of transistor 103 through transistor 104 to VSS. Note

that the claim does not require direct connections), and the gate of the second of the

two NMOS transistors *(Tsuchi, Fig. 1, transistor 104)* is connectable to the first

reference node via a sixth switch of the plurality of switches *(Tsuchi, Fig. 1, VSS is the*

first reference node. As shown in Fig. 3B, during connection 2, switch 120 is ON and

connects the gate of transistor 104 through the same transistor 104 to VSS. Note that

the examiner interpreted the sixth switch to be the same as the fifth switch 120), and the

gate of the first of the two PMOS transistors *(Tsuchi, Fig. 1, transistor 101)* is

connectable, via a seventh switch of the plurality of switches *(Tsuchi, Fig. 1, switch*

111), to a second reference node being biased with a second reference voltage *(Tsuchi,*

Fig. 1, Vdd, which is biased with a high-potential power voltage. As shown in Fig. 3A,

during connection 1, switch 111 is ON and connects the gate of transistor 101 through

transistor 102 to VDD. Note that the claim does not require direct connections) and the

gate of the second of the two PMOS transistors *(Tsuchi, Fig. 1, transistor 102)* is

connectable to the second reference node via an eighth switch of the plurality of

switches *(Tsuchi, Fig. 1, Vdd is the second reference node. As shown in Fig. 3A, during*

connection 1, switch 111 is ON and connects the gate of transistor 102 through the

same transistor 102 to Vdd. Note that the examiner interpreted the eighth switch to be

the same as the seventh switch 111).

6.   Regarding **claim 5**, Tsuchi in view of Sakurai disclose wherein the input stage is

a rail-to- rail input stage (*while Tsuchi does not use the term "rail-to-rail input stage". It*

is obvious that Tsuchi's Fig. 1 is equivalent to the rail-to-rail input stage shown in

Sakurai's Fig.1 per Sakurai's col. 1 lines 22-25. Furthermore, from Tsuchi's Fig. 4, the

differential circuits are being used as 100 rail-to-rail per para. 258).

7.   Regarding **claim 6**, Tsuchi in view of Sakurai disclose wherein the input stage is

configured to keep the NMOS doublet active when the analog input signals are directed

to the second differential input and to keep the PMOS transistor doublet active when the

analog input signals are directed to the first differential (*Tsuchi, Figs. 3A-3B and para.*

147-148. For example, in Fig. 3A, the differential pair is the N-transistors 103 and 104,

and while Tsuchi discloses the P-transistors 101 and 102 "inactive" as a differential pair,

the P-transistors 101 and 102 are "active" as a current mirror. And vice versa for Fig.

3B).

8.   Regarding **claim 7**, Tsuchi in view of Sakurai disclose wherein said switching

signal is a digital switching signal (*as shown in Tsuchi's Fig. 2, the signal is either ON or*

OFF).

9.   Regarding **claim 8**, Tsuchi in view of Sakurai disclose wherein transistors serve

as the switches *(Tsuchi, Fig. 4 per para. 161)*.

10.   Regarding **claim 9**, Tsuchi in view of Sakurai disclose wherein the NMOS

transistor doublet and the PMOS transistor doublet *Tsuchi, Fig. 1)* are part of a folded

cascode rail-to-rail input stage and wherein the folded cascode rail-to-rail input stage is

connected to a second stage comprising a rail-to-rail output stage amplifier *(Tsuchi, Fig.*

1 can be interpreted to be a cascode including the differential pair as the input stage and

the current mirror as the output stage. Also see Fig. 5, where the cascode can be

interpreted as the input stage being all of Fig. 1, and the output stage being the

amplification stages).

11.   Regarding **claim 10**, Tsuchi in view of Sakurai disclose an apparatus comprising:

        a source driver bank with a plurality of input stages *(Fig. 14 per para. 121*

showing a plurality of circuits 100 that drive data lines, in other words, a source driver

bank of a display. They include the amplifier circuits, which include an input stage such

as the one shown in Fig. 1), each input stage *(Fig. 1)* having

        an NMOS transistor doublet *(Fig. 1 and para. 139, N-channel transistors 103 and*

104) having a first differential input *(Fig. 1 and para. 140, VinP and VinM toward*

transistors 103 and 104), for receiving input signals *(Vin per para. 141)*,

a PMOS transistor doublet *Fig. 1 and para. 139, P-channel transistors 101 and 102)* having a second differential input *(Fig. 1 and para. 140, VinP and VinM toward transistors 101 and 102)* for receiving input signals *(Vin per para. 141)*, and

a plurality of switches configured and arranged *(Fig. 1, switches 111-120)*, to, in response to a switching signal *(On or Off signals for connection changeover 1 or connection changeover 2 of Fig. 2)*, direct analog input signals *(supplied through VinP and VinM)* to one of the first and second differential inputs *(Fig. 1 and para. 141)* and to connect the other one of the first and second differential inputs to a reference voltage *(Figs. 3, and para. 141 where one of the pairs acts as a differential input and the other acts as a current mirror clearly connected to VDD or VSS as shown in Figs. 3)*, and

a bus for receiving input signals *(Fig. 14, decoders 300)*.

Tsuchi does not disclose details about the transconductance of the transistors. However, Sakurai discloses the concept of keeping the ratio of the transconductance of the NMOS transistor doublet and the transconductance of the PMOS transistor doublet constant *(Fig. 10, where gmn is the NMOS transistor doublet transconductance and gmp is the PMOS transistor doublet transconductance. In the range from about 0.6Vcm to 1.5Vcm, both gmp and gmp are constant per col. 2 lines 32-36; consequently, their ratio gmn/gmp would be constant. Please note that there are no requirements in the claim to maintain the ratio constant over the whole common mode range)* for a conventional input stage of an Op. Amp *(Sakurai's Fig. 1)*. Thus, it would have been obvious to one of ordinary skill in the art at the time of the invention, given that Tsuchi's differential circuit *(Tsuchi, Fig. 1)* and Sakurai's conventional OpAmp are equivalent

(Sakurai, Fig. 1 and col. 1 lines 11-25, in that both include P-transistors and N-transistors pairs and act as differential input stage. Please note that Sakurai's Fig. 1, Mp1, Mp2, Mn1, Mn2, Ip and In are equivalent to Tsuchi's Fig. 1, 101, 102, 103, 104, 105 and 106), to obtain the predictable result of the ratio of the transconductance of the NMOS transistor doublet and the transconductance of the PMOS transistor doublet to be constant, at least over a region of the common mode voltage (*as taught by Sakurai in Fig. 10 for the range of 0.6Vcm to 1.5Vcm and col. 2 lines 32-36*) in Tsuchi's circuit (*Tsuchi, Fig. 1*). This constant ratio of the transconductances (*as taught by Sakurai*) would be kept constant as a result of the plurality of switches controlling the transistors doublets (*Tsuchi, Fig. 1*) for conventional operation of a differential input stage (*as shown in Tsuchi's Fig. 1 and Sakurai's Fig. 1).*

12.   Regarding **claim 12**, Tsuchi in view of Sakurai disclose further comprising a control signal generator for generating the switching signal (*a control signal generator is required to obtain the changeover control as shown in Tsuchi's Fig. 2*).

13.   Regarding **claim 14**, Tsuchi discloses an apparatus comprising an input stage *(Fig. 1)* with an NMOS transistor doublet *(Fig. 1 and para. 139, N-channel transistors 103 and 104)* having a first differential input *(Fig. 1 and para. 140, VinP and VinM toward transistors 103 and 104)*, for receiving input signals *(Vin per para. 141)*, a PMOS transistor doublet *Fig. 1 and para. 139, P-channel transistors 101 and 102)* having a second differential input *(Fig. 1 and para. 140, VinP and VinM toward transistors 101*

and 102) for receiving input signals *(Vin per para. 141)*, and a plurality of switches *(Fig.*

1, switches 111-120) for receiving and selectively directing analog input signals *(para.*

258 explain that the circuit is used for analog grayscale level voltage. Note that while

they mention Figs. 5, 8, 10 and 12. All of them incorporate the circuit shown in Fig. 1)

only to one of either said first differential input or said second differential input *(para.*

141 explains that either of the P-channel transistor pair or N-channel transistor pair

would operate as the differential pair at a time. Two types of connections are shown in

Figs. 3A-B) responsive to a switching signal *(A changeover signal is required to activate*

the switches 111-120 as required for Figs. 2-3B) and for connecting the other one of the

first and second differential inputs to a reference voltage responsive to the switching

signal *(Figs. 3A-B, where the reference voltages are Vss and Vdd. For example, in Fig.*

3A, when Vin is being supplied to the N-channel transistor pair 103 and 104 as the

differential pair, the P-channel transistor pair is acting as the current mirror and

connected to Vdd and Vss. Vice versa for Fig. 3B) wherein the input stage is configured

to operate in either a first mode *(Fig. 3A)* or a second mode *(Fig. 3B)* responsive to the

switching signal *(per Fig. 2)*, and the NMOS and PMOS transistor doublets are both

kept active in each of the modes *(Figs. 3A-3B and para. 147-148. For example, in Fig.*

3A, the differential pair is the N-transistors 103 and 104, and while Tsuchi discloses the

P-transistors 101 and 102 "inactive" as a differential pair, the P-transistors 101 and 102

are "active" as a current mirror. And vice versa for Fig. 3B), and wherein the plurality of

switches *(Fig. 1, switches 111-120)* are configured, in the first mode *(Fig. 3A)*, to direct

the analog input signals *(Vin)* to the first differential input *(Fig. 1, VinP and VinM toward*

transistors 103 and 104, as shown in Fig. 3A) and to connect a first reference voltage

(Tsuchi, Figs. 1, 3A, VDD), to the second differential input *(Fig. 1, VinP and VinM*

toward transistors 101 and 102. When switch 111 is On in Connection 1 of Fig. 3A,

both 101 and 102 are connected to VDD), and the plurality of switches *(Fig. 1, switches*

111-120) are configured, in the second mode *(Fig. 3B),* to direct the analog input signals

(Vin) to the second differential input *(Fig. 1, VinP and VinM toward transistors 101 and*

102, as shown in Fig. 3B) and to connect a second reference voltage *(Tsuchi, Figs. 1,*

3A, VSS) to the first differential input *(Fig. 1, VinP and VinM toward transistors 103 and*

104. When switch 120 is On in Connection 2 of Fig. 3B, both 103 and 104 are

connected to VSS).

Tsuchi does not disclose details about the transconductance of the transistors.

However, Sakurai discloses the concept of keeping the ratio of the transconductance of

the NMOS transistor doublet and the transconductance of the PMOS transistor doublet

constant *(Fig. 10, where gmn is the NMOS transistor doublet transconductance and*

gmp is the PMOS transistor doublet transconductance. In the range from about 0.6Vcm

to 1.5Vcm, both gmp and gmp are constant per col. 2 lines 32-36; consequently, their

ratio gmn/gmp would be constant. Please note that there are no requirements in the

claim to maintain the ratio constant over the whole common mode range). Thus, it

would have been obvious to one of ordinary skill in the art at the time of the invention,

given that Tsuchi's differential circuit *(Tsuchi, Fig. 1)* and Sakurai's conventional OpAmp

are equivalent *(Sakurai, Fig. 1 and col. 1 lines 11-25, in that both include P-transistors*

and N-transistors pairs and act as differential input stage), to obtain the predictable

result of the ratio of the transconductance of the NMOS transistor doublet and the

transconductance of the PMOS transistor doublet to be constant, at least over a region

of the common mode voltage (*as taught by Sakurai in Fig. 10 for the range of 0.6Vcm to*

1.5Vcm and col. 2 lines 32-36) in Tsuchi's circuit (*Tsuchi, Fig. 1*).

14.   Regarding **claim 15**, Tsuchi in view of Sakurai disclose wherein the first

differential input is formed by the gates of the NMOS transistor doublet *(Tsuchi, Fig. 1*

and para. 140, VinP and VinM toward transistors 103 and 104) and the second

differential input is formed by the gates of the PMOS transistor doublet *(Tsuchi, Fig. 1*

and para. 140, VinP and VinM toward transistors 101 and 102).

15.   Regarding **claims 16 and 17**, Tsuchi in view of Sakurai disclose wherein the

plurality of switches (*Tsuchi, Fig. 1, switches 111-120*) are configured to selectively

direct input signals (*Tsuchi, supplied through VinP and VinM)* to one of the differential

inputs (*Tsuchi, Figs. 1-2 and para. 141*), and to connect the other one of the differential

inputs to a reference voltage (*Tsuchi, Figs. 3, and para. 141 where one of the pairs acts*

as a differential input and the other acts as a current mirror clearly connected to VDD or

VSS as shown in Figs. 3), to keep the transconductance ratio of the NMOS and PMOS

transistor doublets constant (*recall that the transconductance ratio is kept constant upon*

combination with Sakurai for at least a small range when a conventional differential

input stage transconductances of the pMOS and nMOS remain constant, such as

shown in Sakurai's Fig. 10. This occurs as part of the differential operation of an input stage as the one taught by Tsuchi's Fig. 1).

16.   **Claims 11 and 13** are rejected under 35 U.S.C. 103(a) as being unpatentable over Tsuchi in US 2003/0160749 in view of Sakurai et al. in US 5,384,548 as applied above, in further view of common knowledge. Evidence for the official notice can be found below in the Response to Arguments.

17.   Regarding **claim 11**, Tsuchi in view of Sakurai disclose use in a liquid crystal display device (*Tsuchi, para. 181*) but do not explicitly disclose a gate driver bank. However, the examiner takes official notice that it is well known in the art the use of LCDs with gate drivers and data drivers. Thus, it would have been obvious to one of ordinary skill in the art at the time of the invention, to use Tsuchi's in view of Sakurai's with a gate driver bank, in order to obtain the predictable result of enabling operation of a liquid crystal display device (*Tsuchi, para. 181*).

18.   Regarding **claim 13**, Tsuchi in view of Sakurai do not explicitly disclose a panel module. However, the examiner takes official notice that it is well known in the art the use of LCD panels. Thus, it would have been obvious to one of ordinary skill in the art at the time of the invention, to use Tsuchi's in view of Sakurai's apparatus in an LCD panel, because Tsuchi already discloses that one of his applications is a display circuit (*para. 121*) of a liquid crystal display device (*Tsuchi, para. 181*).

19.   **Claim 2** is rejected under 35 U.S.C. 103(a) as being unpatentable over Tsuchi in

US 2003/0160749 in view of Sakurai et al. in US 5,384,548 as applied above, in further

view of Nishimura in US 2001/0004255.

Tsuchi in view of Sakurai disclose wherein the plurality of switches (*Tsuchi's Fig.*

1, switches 111-120) direct the analog input signals (*supplied through VinP and VinM)*

to said first differential input *(Tsuchi's Fig. 1, VinP and VinM toward transistors 103 and*

104) if the input signals have positive data (*Tsuchi, para. 185 and Fig. 7 referring to high*

potential level VL1 in state 1 shown in Fig. 3A) and to said second differential input

(Tsuchi's Fig. 1, VinP and VinM toward transistors 101 and 102) if the input signals

have negative data (*Tsuchi, para. 185 and Fig. 7 referring to low potential level VL2 in*

state 2 shown in Fig. 3B). Tsuchi in view of Sakurai further disclose the use of the

circuit for grayscale voltage level in a liquid crystal display *(Tsuchi's para. 2, 15-17)*, but

fail to explicitly disclose the voltages to be gamma data. However, Nishimura discloses

the well known concept of using gamma corrected picture signals on an LCD

(Nishimura, para. 7). Thus, it would have been obvious to one of ordinary skill in the art

at the time of the invention to use gamma corrected data for grayscale level voltage of

Tsuchi, in order to obtain the predictable result of gamma correcting signals for use in

LCDs to improve user experience.

Response to Arguments

20.   Applicant's arguments filed 1/14/2011 have been fully considered but they are

not persuasive. On the Remarks pg. 6-7, the Applicants argue with respect to **claim 1**,

that Sakurai ('548) does not disclose keeping a transconductance ratio of NMOS and

PMOS transistor doublet constant, and that it is unclear how Tsuchi ('749) would be

modified to meet This teaching by Sakurai. On the Remarks pg. 8, the Applicants

continue to argue that the '548 reference does not use any switches to control

transconductance but uses dynamic bias control.

The examiner must respectfully disagree. As cited in the rejection above,

Sakurai teaches a conventional input stage (*Sakurai, Fig. 1*) which is equivalent to

Tsuchi's (*Tsuchi, Fig. 1*) in that both include P-transistors and N-transistors and act as

differential input stages. The whole background of the Invention in Sakurai discloses

the issues that are observed with a differential input stage as the one disclosed in

Sakurai's Fig. 1 (*which is equivalent to Tsuchi's Fig. 1*) and clearly explain that in such

circuit, the transconductance of the n-type FETs and the p-type FETs (*right side of the*

equation 3 in Sakura's col. 2 per col. 1 lines 45-50) is constant for only a small region of

the common mode range (*Sakurai, col. 2 lines 32-36*).   Please note that neither of the

claims require <u>the ratio of the transconductance to remain constant during a specific</u>

<u>range</u>, and as such, even the teaching of keeping the n-type FETs and p-type FETs

constant during a small region, results in a constant transconductance ratio during a

small region (as shown in Sakurai's Fig. 10, but described in col. 2 lines 32-36).

Because Sakurai is describing the issues found with a differential input stage which

includes the same switches configuration for the pMOS and nMOS doublets as Tsuchi's

Fig. 1, it would have been obvious to one of ordinary skill in the art at the time of the

invention that Tsuchi's differential input stage will have the predictable result (*because*

the two cited parts of the references are equivalent) of a constant ratio of

transconductances during at least a small region (as taught by Sakurai). Also note that

the dynamic control bias for keeping the transconductances constant was not used for

the rejection, but the conventional operation described in Sakurai's background of the

invention. For further clarification, please note that Sakurai's Fig. 1, Mp1, Mp2, Mn1,

Mn2, Ip and In are equivalent to Tsuchi's Fig. 1, 101, 102, 103, 104, 105 and 106.

The Applicant also argues with respect to **claim 2**, on the Remarks pg. 8, that

Nishimura ('255) fails to disclose the switches operating based on the presence of

positive or negative gamma data. The examiner must again respectfully disagree,

please note that Tsuchi already discloses the use of his circuit to include amplifier

circuits for grayscale level voltage of an LCD (*para. 2, 15-16*) and Nishimura clearly

discloses the use of gamma correction for LCDs using amplifier for voltage generation

(*Nishimura, Fig. 1 and para. 7*), thus, it would have been obvious to one of ordinary skill

in the art at the time of the invention, that Tsuchi's invention can be used after gamma

correction, and thus the voltages received by a differential input stage (*as taught by*

Tsuchi) of an Op. Amp will be gamma corrected voltages (*Nishimura, para. 7*).

The examiner corrected a typographical error in claim 2 above for better

readability, but the rejection remains the same.

Finally, the Applicants request to provide evidence with respect to the official

notice taken for the rejections of **claims 11 and 13**. Please see Udo et al. in US

2002/0008684 (*Fig. 2, bank of drivers 16 and 18 of LCD panel per para. 4*), Youn in US

2002/0089485 also teaching an LCD panel (*Fig. 3, bank of drivers 200 and 400*), and

Goto et al. in US 2002/0171613 (*Fig. 1, bank of drivers 140, 131 of LCD panel 10*).

Conclusion

21.   **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time

policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE

MONTHS from the mailing date of this action. In the event a first reply is filed within

TWO MONTHS of the mailing date of this final action and the advisory action is not

mailed until after the end of the THREE-MONTH shortened statutory period, then the

shortened statutory period will expire on the date the advisory action is mailed, and any

extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of

the advisory action. In no event, however, will the statutory period for reply expire later

than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the

examiner should be directed to LILIANA CERULLO whose telephone number is

(571)270-5882. The examiner can normally be reached on Monday to Thursday 9AM-

4PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's

supervisor, Amr Awad can be reached on 571-272-7764. The fax phone number for the

organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the

Patent Application Information Retrieval (PAIR) system. Status information for

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Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a

USPTO Customer Service Representative or access to the automated information

system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/L. C./
Examiner, Art Unit 2629

/Amr Awad/
Supervisory Patent Examiner, Art Unit 2629